Specification of the Layer 0 Hybrid for the upgraded D0 Silicon Microstrip Detector (Part 3823-112-EB-330378 Rev. B2)

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Overview

The hybrid is to be constructed of alternating thick film layers of gold and dielectric built up onto a Beryllia substrate. There are six conductor layers and five dielectric layers on the top side. In addition to these layers, a strip of conductor is to be applied to the back side as per the files provided and this strip is to be grounded by means of three holes drilled through the substrate. The top metal layer will consist of two different finishes. Some pads will be compatible for aluminum-wedge bonding while other pads must be solderable. The solderable layer will be represented by a separate layer drawing. The layout of all the layers is defined in both .dxf format and Gerber and accompany this specification together with a general hybrid drawing.

Specifications

Dimensions and Flatness

1. Laser cutting should produce a final outline of 35mm +/-0.05mm by 17.9mm +/-0.05mm (1.378" +/- 0.002" by .705" +/- 0.002"). Cut edge location should be accurate to +/-0.05mm (+/- 0.002") to the overall artwork pattern, Layer 1 Conductor Top. A Fiducial mark will be referenced to aid in accomplishing this alignment. See drawing 3823.000-MB-399425.
2. Total thickness of the finished hybrid must not exceed 0.85mm (33.46mil) (i.e. the hybrid should lie between two parallel planes separated by not more than 0.85mm)
3. Flatness of the top and bottom surfaces of the finished hybrid must be within 0.15 mm (i.e. all points on the surface lie between two parallel planes separated by 0.15 mm or less)
4. Minimum thickness of the 99.5% BeO substrate is 0.305mm (12 mil)

Electrical

5. Dielectric layer thickness is to be 25 um (1 mil) minimum, with a dielectric strength of 500V/mil or better.
6. Thickness of metal trace layers is recommended to be 6 um (0.236 mil) minimum, 10 um (.394 mil) maximum.
7. Flying Probe resistance measurements for all nets for each hybrid is requested. The output can be hard copy or files. As a minimum requirement, resistance measurements of the clock lines is to be made, and the resistance of the clock lines is to be smaller than 6 Ohms. See section "Resistance Measurement of Clock Lines" below.
8. Vendor must test 100% all nets for continuity, which includes opens and shorts
9. Ground and power plane layer thickness is to be 4 um (0.157mil) minimum, 8 um (0.315 mil) maximum..

Miscellaneous

10. Bond pads should be thick film gold formulated for aluminum wedge bonding with a typical thickness of 7-11um (0.275-0.433 mil).
11. Solder pads should be of Platinum Palladium Gold Pt/Pd/Au with a minimum thickness of 15um and should be formulated for soldering with Sn62 solder.
12. Surface area under each of the two SVX chips must be conductive, open on the solder mask layer and should accept silver epoxy.
13. Soldermask on vias is preferred.
14. Silkscreen is to be applied for component identification
15. The ground strip on the back side of the substrate should be 2mm wide and extend the full length of the hybrid on the right side when looking from the bottom. See layer "Bot Ceramic GND layer." Deposition should be between 6 and 10 um and should be gold.
16. The three vias drilled through the substrate are defined on the "Drill Thru Ceramic Layer" and should be .005" to .012" in diameter.
17. Dielectric printing on the backside of the beryllia for the purpose of maintaining flatness is allowed, except on the outermost 2mm of either vertical edge.

Standards of Testing shall be according to these Mil-Specs

Vendor must adhere to standards of fabrication and testing as described in the following specs.

- MIL-STD 883E Method 2011.7 Bond Strength (Destructive Bond Pull Test)
- MIL-STD 977 Method 4500 Metalization Adherence (Tape Test)
- MIL_STD_883E Method 2019.5 Die Shear Strength

Documentation

Vendor should provide a Quality Inspection Test document for each lot of product that is manufactured.

This document should provide tests and procedure references as follows:

• Visual inspection	Test sample 100%
• Physical Dimensions (including thickness)	Test sample 100%
• Electrical Tests	Test Sample 100%
• Film Adhesion	Test sample 5% but at least two pieces.
• Wirebond Evaluation	Test Sample 5% but at least two pieces.
• Die Shear	Test Sample 5% but at least two pieces.
• Solder Pad Evaluation	Test Sample 5% but at least two pieces.
• Warp and Camber	Test Sample 10% but at least four pieces.
• Glue channel depth	Test Sample 5% but at least two pieces.

Beryllia (Beo) Decontamination and Handling

Fermilab standards require that the hybrids be decontaminated for Beryllia dust. Vendor should thoroughly wash with hot water, rinse with alcohol and handle the hybrid to assure minimal beryllia dust contamination.

Vendor can verify his decontamination process through this third party source.

Consult Natlsco Loss Control of Long Grove for further details.

1 Kemper Dr, Long Grove, IL 60049
Bill Walsh 847.320.7188

Resistance Measurement of Clock Lines
Two lines are to be measured for proper maximum resistance, CLK, and /CLK. The table below shows coordinate locations for either end of these nets. Resistance for each line is to be 1.2 ohms maximum.

Net	ProbeA (inches)	ProbeB (inches)	ProbeA (mm)	ProbeB (mm)
CLK	(.114, .260)	(.513, .815)	(2.9, 6.6)	(13.03, 20.7)
/CLK	(.134, .260)	(.505, .815)	(3.4, 6.6)	(12.83, 20.7)

Delivery Schedule

- Partial deliveries are accepted.

Contacts

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Build Files Gerber And AutoCad

Manufacturing Files contained in L0_hybrid_revb2_020604pm_mfr.zip

- Note Gerber files 274X extension *.GDO
- AutoCAD files in DXF format R12
- Layer 3 Dielectric is used multiple times between Layers 1,2; 2,4; 4,5; 5,6; Layer 7 is between Layers 6,8.
- Note that Layer 8 is closest to the substrate
- Bot_Ceramic Layer is on the backside of the substrate.
- Drill_substrate defines the drilling of substrate for the backside connecting vias.
- * Reference files.

Directory of L0_hybrid_revb2_020604pm_mfr.zip (02/12/2004 08:15a 4,336K)

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02/06/2004  02:44p           173,104 GenSilkTop.gdo
02/06/2004  03:32p         9,852,327 L0_hybrid_revb2_020604pm_sst.dxf
02/06/2004  02:44p            47,661 SldrmskTop.gdo
02/06/2004  03:30p         2,365,969 L0_hybrid_revb2_020604pm_smt.dxf

02/06/2004  02:44p            48,230 Lyr1Top_bond.gdo
02/06/2004  03:36p         2,365,302 L0_hybrid_revb2_020604pm_lyr1TBond.dxf
02/06/2004  02:44p            50,532 Lyr1Top_solder.gdo
02/06/2004  03:38p         2,464,911 L0_hybrid_revb2_020604pm_lyr1TSld.dxf

02/06/2004  02:44p           143,509 Lyr1Top_Traces.gdo
02/06/2004  03:34p         5,913,880 L0_hybrid_revb2_020604pm_lyr1TT.dxf
02/06/2004  02:44p            44,997 Lyr2.gdo
02/06/2004  03:41p         2,212,046 L0_hybrid_revb2_020604pm_lyr2.dxf

02/06/2004  02:44p           105,797 Lyr3.gdo
02/06/2004  03:43p         5,485,945 L0_hybrid_revb2_020604pm_lyr3.dxf
02/06/2004  02:44p            44,559 Lyr4.gdo
02/06/2004  03:45p         2,217,201 L0_hybrid_revb2_020604pm_lyr4.dxf

02/06/2004  02:44p           171,437 Lyr5.gdo
02/06/2004  03:47p         6,721,628 L0_hybrid_revb2_020604pm_lyr5.dxf
02/06/2004  02:44p            45,795 Lyr6.gdo
02/06/2004  03:48p         2,272,067 L0_hybrid_revb2_020604pm_lyr6.dxf

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02/06/2004  03:50p         2,544,646 L0_hybrid_revb2_020604pm_lyr7.dxf
02/06/2004  02:44p            78,292 Lyr8Bottom.gdo
02/06/2004  03:51p         3,616,746 L0_hybrid_revb2_020604pm_lyr8bot.dxf

02/06/2004  02:44p            59,070 Bot_Ceramic.gdo
02/06/2004  03:53p         3,189,534 L0_hybrid_revb2_020604pm_botcer.dxf
02/06/2004  02:44p            62,234 Drill_Substrate.gdo
02/06/2004  03:54p         3,384,245 L0_hybrid_revb2_020604pm_drlsub.dxf

* 02/06/2004  02:44p            39,991 PasteTop.gdo
* 02/06/2004  03:28p         2,050,825 L0_hybrid_revb2_020604pm_spt.dxf
* 02/06/2004  02:44p            50,115 Assembly.gdo
* 02/06/2004  03:26p         2,921,357 L0_hybrid_revb2_020604pm_assem.dxf
* 02/06/2004  02:44p            50,113 AssyTop.gdo
* 02/06/2004  03:27p         2,890,650 L0_hybrid_revb2_020604pm_ast.dxf

02/12/2004    09:56a          130,280   L0_MB399425.dwg (Substrate Mechanical cut
                                        outline)
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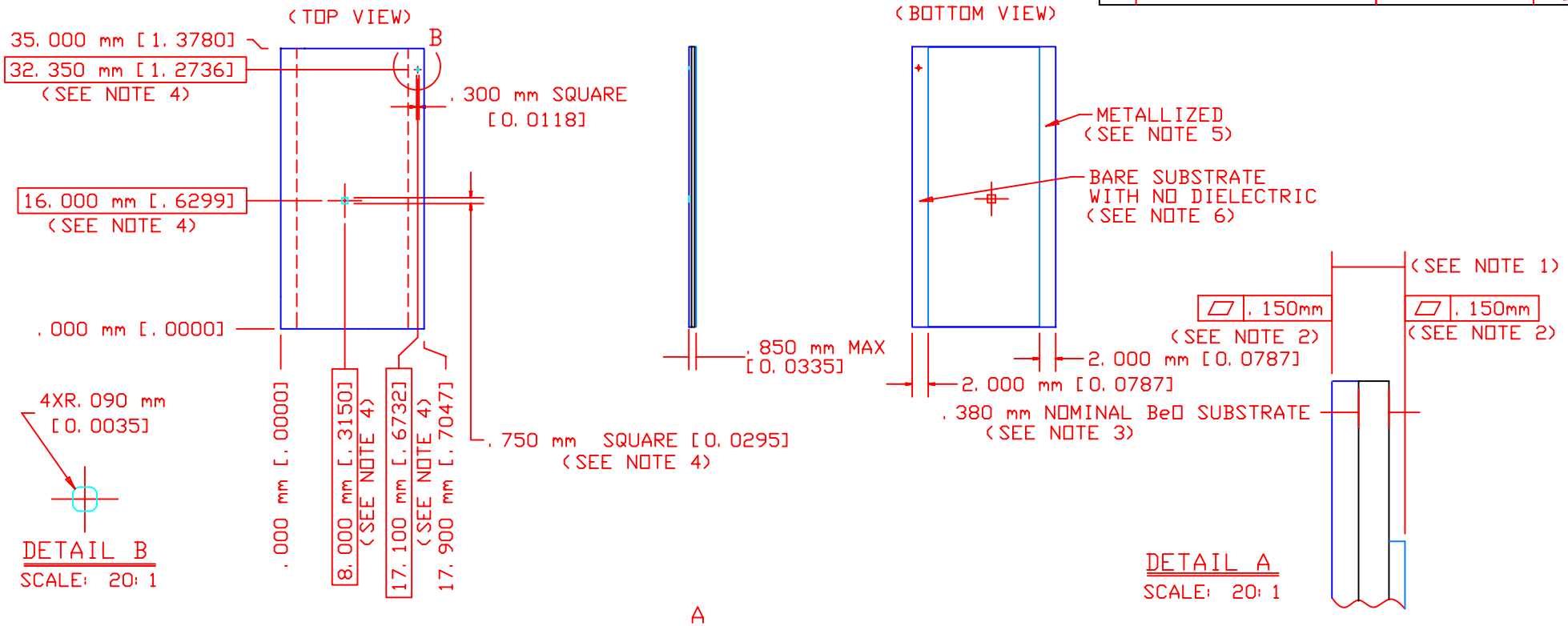
REV	DESCRIPTION	DRAWN	DATE
		APPROVED	DATE



NOTES:

1. COMPLETED PART MUST FIT BETWEEN TWO PARALLEL PLANES SEPARATED BY .850 mm.
2. PRINTED PORTIONS OF TOP & BOTTOM SURFACES ARE TO BE FLAT TO .150 mm (MEANING THAT ALL POINTS ON THESE REGIONS OF A SURFACE LIE BETWEEN PARALLEL PLANES SEPARATED BY NOT MORE THAN .150 mm).
3. BeO SUBSTRATE 0.305mm MINIMUM THICKNESS.
4. NOMINAL LOCATIONS OF REFERENCE FEATURES FOR CUT EDGE TO TOP METAL LAYER ALIGNMENT.
5. METALLIZATION APPROPRIATE FOR SILVER EPOXY JOINT. TOTAL METAL THICKNESS APPROXIMATELY 0.01 mm. MATERIAL & THICKNESS TO BE PROPOSED BY VENDOR & APPROVED BY FERMILAB.
6. DIELECTRIC PRINTING FOR PURPOSE OF MAINTAINING FLATNESS.

UNLESS OTHERWISE SPECIFIED			ORIGINATOR	W. E. COOPER	21-MAR-2002
.XX	.XXX	ANGLES	DRAWN	F. BROWNING	21-MAR-2002
± .05mm	± .05mm	± 1°	CHECKED	M. HRYCYK	12-FEB-2004
1. BREAK ALL SHARP EDGES .40mm. 2. DO NOT SCALE DRAWING. 3. DIMENSIONS BASED UPON ANSI Y14.5M-1982 4. ALL DIMENSIONS ARE MILLIMETERS [INCHES] 5. MAX. ALL MACH. SURFACES 3.2			APPROVED	W. E. COOPER	12-FEB-2004
			USED ON	MC-399896	
			MATERIAL		

FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY

DO-SILICON RUN2B 2 CHIP HYBRID SUBSTRATE MECHANICAL CUT OUTLINE

SCALE	DRAWING NUMBER	SHEET	REV
2:1	3823.000-MB-399425	1 OF 1	

CREATED WITH: Ideas9m3 GROUP: PPD/MECHANICAL DEPARTMENT